REMARKS

I. Introduction

Claims 1, 3-10 and 12 are currently pending. Claims 1 and 12 have been amended. The amendments to the claims do not add new matter, and the amendments are made in order to comply with the Examiner's requirements. Accordingly, entry of the amendments is requested. In view of the foregoing amendments and the following remarks, it is respectfully submitted that all of the presently pending claims are in allowable condition.

II. Drawings

The Examiner has indicated that the previously submitted replacement drawing of Figure 2 has been approved, but the Examiner has also indicated that the labels in the replacement drawing are illegible in places, and therefore the drawing is not acceptable as a replacement sheet. In response, a new replacement sheet including Fig. 2 is submitted herewith. Acceptance of the new replacement sheet is respectfully requested.

III. Objections to the Claims

The Examiner has objected to claims 1 and 3-9 on the grounds that in the phrase "activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor and then transmitted to the JTAG interface" is ambiguous since no action is carried out prior to the "then" clause and it is unclear after what action the test routine is transmitted. Without passing judgment on the merits of this objection, claim 1 has been amended to recite "transmitting a test data stream provided by the test routine to the JTAG interface."

In response to the Examiner's objection to claim 12, Applicants have amended claim 12 in accordance with the Examiner's suggestion.

It is therefore submitted that the objections to the claims have been obviated. Withdrawal of the objections to the claims is accordingly respectfully requested.

IV. Rejection of Claims 1 and 3-9 under 35 U.S.C. § 112, second ¶

Claims 1 and 3-9 were rejected under 35 U.S.C. § 112, second ¶, as being indefinite for essentially the same reasons asserted in connection with the objection to claims 1 and 3-9 addressed above. Since claim 1 has been amended to recite "transmitting a test data stream provided by the test routine to the JTAG interface," it is submitted that the indefiniteness rejection has been obviated and that claims 1 and 3-9 are definite. Withdrawal of the indefiniteness rejection of claims 1 and 3-9 is accordingly respectfully requested.

V. Rejection of Claims 1-8 and 10-12 under 35 U.S.C. § 102(b)

Claims 1, 3 to 8, 10 and 12 were rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,724,505 to Argade et al. ("Argade"). Applicants respectfully submit that Argade does not anticipate claims 1, 3-8, 10 and 12, for the following reasons.

In order to reject a claim under 35 U.S.C. §102, the Office must demonstrate that each and every limitation is identically disclosed in a single prior art reference. See Scripps Clinic & Research Foundation v. Genentech, Inc., 18 U.S.P.Q.2d 1001, 1010 (Fed.Cir. 1991). The identical invention must be shown in as complete detail as is contained in the claim. MPEP §2131.

Amended claim 1 recites the steps of activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor and **transmitting a test data stream provided by the test routine to the JTAG interface from the microprocessor**, wherein I/O ports of the microprocessor are connected to pins of the JTAG interface, and a data-in pin of the JTAG interface is activated using the test routine via the I/O ports. It is submitted that Argade does not identically disclose each of these features of claim 1.

As explained in the specification, the present invention proposes a modification of the microprocessor so that the JTAG interface can be activated by a test routine that is executable on the microprocessor. (See Specification, page 7, lines 20-23). Thus, as claimed, the microprocessor both executes a test routine and

transmits a test data stream provided by the test routine to the JTAG interface. Thus, the microprocessor itself initiates and controls the JTAG boundary scan procedure by providing the test routine and the associated test data stream, thereby eliminating the need for access to the JTAG interface from an external controller device – a particularly important feature in embedded devices in which direct I/O access to the JTAG interface is infeasible.

Argade, in contrast, does not disclose (or even suggest) a microprocessor executing a test routine or transmitting a test data stream provided by the test routine to a JTAG interface. In Argade, an ***external*** debug host computer (100) controls the JTAG test procedure: "A [JTAG] interface . . . coupled to the processor core 12, is provided for interpreting JTAG signals *received from an external debug host computer 100.*" (Argade, col. 4, lines 44-47; emphasis added). In fact, Argade merely uses the JTAG interface as a serial port for scanning out a trace of instructions to the debugging host computer. (See Argade, col. 4, lines 63-65).

Since Argade does not identically disclose "activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor and transmitting a test data stream provided by the test routine to the JTAG interface from the microprocessor," claim 1 and its dependent claims 3-8 are not anticipated by Argade. Since independent claim 10 recites features analogous to those of claim 1, it is submitted that claim 10 and its dependent claim 12 are also not anticipated by Argade.

In view of the above, withdrawal of the anticipation rejection of claims 1, 3-8, 10 and 12 is accordingly requested.

VI. Rejection of Claim 9 under 35 U.S.C. § 103(a)

Claim 9 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Argade in view of U.S. Patent 5,357,432 to Margolis et al. ("Margolis").

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie

obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

Claim 9 depends from, and incorporates the limitations of, claim 1. The Margolis reference merely refers to an automatic guidance control system that includes a microcontroller. As discussed in the Amendment responsive to the previous Office Action, Margolis does not in any way refer to a boundary scan procedure according to IEEE 1149, let alone refer to specific ways of implementing such a procedure. As such, Margolis fails to cure the critical deficiencies of the primary Argade reference discussed above with respect to claim 1. Therefore, the combination of Argade and Margolis references does not disclose or suggest all features of claim 1, from which claim 9 depends. For at least these reasons, claim 9 is not rendered obvious by Argade and Margolis.

Withdrawal of the obviousness rejection of claim 9 is therefore respectfully requested.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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